

WSG300S Sigfox Verified Module (RC2/4)

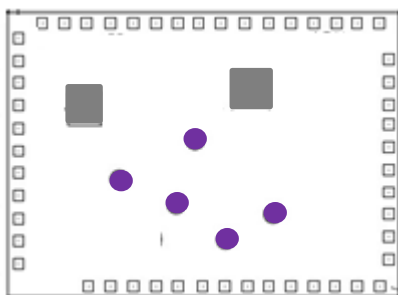
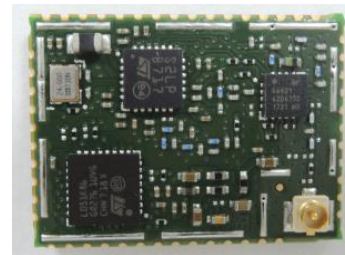
RF Output Power Up To +22dBm (Sigfox)

WSG300S RC24 is a Sigfox modem module for the low power wide area network (LPWAN) market. It is designed with STM's system S2-LP+STM MCU+Sky66421 for the US or other FCC-like market (FCC Part 15.247). The module was designed for high performance, high quality, low cost, small form factor and most importantly, high RF power of up to 22dBm. The design is fully compliant to FCC regulations. The Sigfox application is running on STM32 MCU at high efficiency using its internal 32bit core Cortex-M0 processor. Every module is preloaded with Sigfox application software, module specific ID/KEY/PAC as referring to Sigfox network system. The preloaded software also includes a bootloader which allows software update or future user application development.

(Pin to pin compatible with WSG303S RC1 Module)

Features

- Operating Frequency: ISM RC2 (902MHz) and RC4 (920MHz)
- Sigfox compliant AT command set via UART
- Maximum transmission power: 22dBm
- Current consumption:
 - 184mA Tx at 22dBm (Peak current with Sigfox packet transmission)
 - 4.7uA at sleep mode
- Small-form-factor
 - 16.5x22.5mm stamp package
 - Compact board design with low external component counts
- Voltage supply : 2.0V ~ 3.6V
- 64KB Flash & 8KB RAM Embedded
- Operation Temperature: -40C ~ 85C
- FCC Part 15.247
- Preloaded Sigfox application with ID/KEY/PAC and bootloader for firmware update
- Evaluation kit available



Pinout (bottom view)

- Thermal pad
- Test pad

Pin [Ⓟ]	Pin Define [Ⓟ]	Status [Ⓟ]	Description [Ⓟ]
1,2,3,4,5,15,16,19,40,41,42,43,44,45,47,48,49,50,51,52,53 [Ⓟ]	GND [Ⓟ]	GND [Ⓟ]	Pin 52, 53 Thermal pad [Ⓟ]
6 [Ⓟ]	SDO [Ⓟ]	SPI1_MISO [Ⓟ]	PA6 [Ⓟ]
7 [Ⓟ]	SDI [Ⓟ]	SPI1_MOSI [Ⓟ]	PA7 [Ⓟ]
8 [Ⓟ]	SCLK [Ⓟ]	SPI1_SCK [Ⓟ]	PB3 [Ⓟ]
9 [Ⓟ]	CSN [Ⓟ]	I/O [Ⓟ]	PA1 [Ⓟ]
10 [Ⓟ]	GPIO0 [Ⓟ]	I/O [Ⓟ]	PA0 [Ⓟ]
11 [Ⓟ]	GPIO1 [Ⓟ]	I/O [Ⓟ]	PA4 [Ⓟ]
12 [Ⓟ]	GPIO2 [Ⓟ]	I/O [Ⓟ]	PB1 [Ⓟ]
13 [Ⓟ]	GPIO3 [Ⓟ]	I/O [Ⓟ]	PA15 [Ⓟ]
14 [Ⓟ]	SDN [Ⓟ]	I/O [Ⓟ]	SDN=0, Shutdown mode [Ⓟ]
17 [Ⓟ]	USART_TX [Ⓟ]	O [Ⓟ]	PA2 (115200bps) [Ⓟ]
18 [Ⓟ]	USART_RX [Ⓟ]	I [Ⓟ]	PA3 (115200bps) [Ⓟ]
19 [Ⓟ]	PA5 [Ⓟ]	I/O [Ⓟ]	PA5 [Ⓟ]
20 [Ⓟ]	PB0 [Ⓟ]	EVENTOUT [Ⓟ]	PB0 [Ⓟ]
21 [Ⓟ]	PB2 [Ⓟ]	LPTIM1_OUT [Ⓟ]	PB2 [Ⓟ]
22 [Ⓟ]	PA9 [Ⓟ]	I/O [Ⓟ]	PA9 [Ⓟ]
23 [Ⓟ]	PA10 [Ⓟ]	I [Ⓟ]	PA10 [Ⓟ]
24 [Ⓟ]	PA11 [Ⓟ]	I/O [Ⓟ]	PA11 [Ⓟ]
25 [Ⓟ]	PA12 [Ⓟ]	I/O [Ⓟ]	PA12 [Ⓟ]
26 [Ⓟ]	SWDIO [Ⓟ]	I [Ⓟ]	PA13 [Ⓟ]
27 [Ⓟ]	SWCLK [Ⓟ]	I [Ⓟ]	PA14 [Ⓟ]
28 [Ⓟ]	PA15 [Ⓟ]	I/O [Ⓟ]	PA15 [Ⓟ]
29 [Ⓟ]	PB4 [Ⓟ]	I/O [Ⓟ]	PB4 [Ⓟ]
30 [Ⓟ]	PB5 [Ⓟ]	I/O [Ⓟ]	PB5 [Ⓟ]
31 [Ⓟ]	PB6 [Ⓟ]	I/O [Ⓟ]	PB6 [Ⓟ]
32 [Ⓟ]	PB7 [Ⓟ]	I/O [Ⓟ]	PB7 [Ⓟ]
33 [Ⓟ]	NRST [Ⓟ]	I [Ⓟ]	NRST [Ⓟ]
34 [Ⓟ]	BOOT0 [Ⓟ]	BOOT0 [Ⓟ]	BOOT0 [Ⓟ]
35 [Ⓟ]	PB8 [Ⓟ]	I2C1_SCL [Ⓟ]	PB8 [Ⓟ]
36 [Ⓟ]	XI [Ⓟ]	OSC32_IN [Ⓟ]	PC14-OSC_IN [Ⓟ]
37 [Ⓟ]	XO [Ⓟ]	OSC32_OUT [Ⓟ]	PC15-OSC32_OUT [Ⓟ]
38 [Ⓟ]	VDD [Ⓟ]	VDD [Ⓟ]	VDD_3V3 [Ⓟ]
46 [Ⓟ]	ANT1 [Ⓟ]	I/O [Ⓟ]	SigFox Antenna [Ⓟ]

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Functional Block Diagram

